capacitors. If the capacitors C1, C2, C3, C4 all have the same capacitance value C, then the charge is shared equally so that the voltage across each capacitor becomes $V_{ref}/2$. Referring now to FIG. 33C, on phase P2 of the 3-phase clock (FIG. 32), switch S200 is in the closed condition because P2 has a logic state 1 and bit_1 has a logic state 1. Switch S201 is in the closed condition because P2 has a logic state 1 and bit_2 has a logic state 1. Switches S202, S203 are in the open condition because bit_3, bit_4 have a logic state 0. Output switch S204 is in the closed condition, and capacitors C1 and C2 (FIG. 31) of one-bit DACs 162, 164 delivers charge to the output terminal 510. Consequently, the total charge delivered to the output terminal 510 is equal to C*Vref.

In the Claims:

Please amend the claims as follows. Applicants have attached marked-up claims on a separate page, with deletions and additions to the text indicated by bracketing and underlining, respectively.

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1. (Amended) A system comprising:

a DAC that receives a multi-bit digital signal and outputs at least two analog signals including a first analog signal and a second analog signal, the first analog signal being indicative of a sum of values of bits in the multi-bit digital signal, the second analog signal also being indicative of said sum of values of said bits in the multi-bit digital signal; and

a signal conditioning stage that receives at least two of the at least two analog signals, including the first analog signal and the second analog signal.

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5. (Amended) A system comprising:

a DAC that receives a sequence of digital input signals at an input data rate and outputs a sequence of analog signals to a signal conditioning stage at an output data rate, each of the analog signals being indicative of an associated one of the digital input signals, the magnitude of the output data rate being different than the magnitude of the input data rate, wherein more than one of the analog signals is generated during a single digital to analog conversion cycle of the DAC.

6. (Amended) The system of claim 5 wherein the signal conditioning stage comprises a switched capacitor filter stage.

AS Cont'd

7. (Amended) The system of claim 5 wherein the DAC comprises a switched capacitor DAC.

8. (Amended) The system of claim 5 wherein the magnitude of the output data rate of the DAC is at least twice the magnitude of the input data rate of the DAC.

9. (Amended) The system of claim 5 wherein the magnitude of the output data rate of the DAC is two times the magnitude of the input data rate of the DAC.

10. (Amended) The system of claim 5 wherein the signal conditioning stage generates a signal responsive to the sequence of analog signals.

11. (Amended) The system of claim 5 wherein the DAC receives one digital input signal per operating cycle and the analog signals are output at a non periodic rate over the operating cycle.

12. (Amended) The system of claim 11 wherein the analog signals have a periodic effect on an output of the signal conditioning stage.

13. (Amended) A method comprising:

receiving a multi-bit digital signal;

generating at least two analog signals including a first analog signal that is indicative of a sum of values of bits in the multi-bit digital signal, and a second analog signal that is indicative of said sum of values of said bits in the multi-bit digital signal; and

filtering at least two of the at least two analog output signals, including the first analog signal and the second analog signal.

14. (Amended) The method of claim 13 wherein the at least two analog signals are substantially equal to one another.

A5 cont

15. (Amended) The method of claim 13 wherein the filtering comprises providing the at least two of the at least two analog signals to a switched capacitor filter.

A6

17. (Amended) A system comprising:

means for receiving a multi-bit digital signal;

means for generating at least two analog signals including a first analog signal that is indicative of a sum of values of bits in the multi-bit digital signal, and a second analog signal that is indicative of said sum of values of said bits in the multi-bit digital signal; and

means for filtering at least two of the at least two analog signals, including the first analog signal and the second analog signal.

18. (Amended) The system of claim 17 wherein the at least two analog signals are substantially equal to one another.

A7

20. (Amended) The system of claim 17 wherein the means for generating comprises a switched capacitor DAC.

Please add the following claims:

A8

21. (New) The system of claim 1 wherein the first analog signal and the second analog signal are each indicative of a sum of values of all of the bits in the multi-bit digital signal.

22. (New) The system of claim 1 wherein the first analog signal and the second analog signal are substantially equal to each other.

23. (New) The system of claim 1 wherein the first analog signal and the second analog signal are not substantially equal to each other.

24. (New) The system of claim 1 wherein the at least two analog signals are each indicative of said sum of values of said bits in the multi-bit digital signal.

25. (New) The system of claim 1 wherein each of the at least two analog signals is indicative of a sum of values of all of the bits in the multi-bit digital signal.

26. (New) The system of claim 1 wherein the at least two analog signals are not all substantially equal to each other.

27. (New) The system of claim 1 wherein the signal conditioning stage generates a signal that is responsive to both the first analog signal and the second analog signal.

28. (New) The system of claim 1 wherein the signal conditioning stage generates a signal that is responsive to each of the at least two of the at least two analog signals.

29. (New) A method comprising:

receiving a multi-bit digital signal;

generating at least two analog signals including a first analog signal that is indicative of a sum of values of bits in the multi-bit digital signal, and a second analog signal that is indicative of said sum of values of said bits in the multi-bit digital signal; and

providing at least two of the at least two analog signals to a signal conditioning stage, the at least two of the at least two analog signals including the first analog signal and the second analog signal.

30. (New) The method of claim 29 wherein the first analog signal and the second analog signal are each indicative of a sum of values of all of the bits in the multi-bit digital signal.

31. (New) The method of claim 29 wherein the first analog signal and the second analog signal are substantially equal to each other.

32. (New) The method of claim 29 wherein the first analog signal and the second analog signal are not substantially equal to each other.

33. (New) The method of claim 29 wherein the at least two analog signals are each indicative of said sum of values of said bits in the multi-bit digital signal.

34. (New) The method of claim 29 wherein the at least two analog signals are each indicative of a sum of values of all of the bits in the multi-bit digital signal.

35. (New) The method of claim 29 wherein the at least two analog signals are substantially equal to each other.

36. (New) The method of claim 29 wherein the at ieast two analog signals are not substantially equal to each other.

37. (New) A method as in any of claims 13 or 29, further comprising generating a signal that is responsive to both the first analog signal and the second analog signal.

38. (New) A method as in any of claims 13 or 29, further comprising generating a signal that is responsive to each of the at least two of the at least two analog signals.

39. (New) A system comprising:

means for generating at least two analog signals in response to a multi-bit digital signal, the at least two analog signals including a first analog signal that is indicative of a sum of values of bits in the multi-bit digital input signal and a second analog signal that is indicative of said sum of values of said bits in the multi-bit digital signal; and

a signal conditioning stage that receives at least two of the at least two analog signals, including the first analog signal and the second analog signal.

40. (New) The system of claim 39 wherein the first analog signal and the second analog signal are each indicative of a sum of values of all of the bits in the multi-bit digital signal.

41. (New) The system of claim 39 wherein the first analog signal and the second analog signal are substantially equal to each other.

42. (New) The system of claim 39 wherein the first analog signal and the second analog signal are not substantially equal to each other.

43. (New) The system of claim 39 wherein the at least two analog signals are each indicative of said sum of values of said bits in the multi-bit digital signal.

44. (New) The system of claim 39 wherein the at least two analog signals are each indicative of a sum of values of all of the bits in the multi-bit digital signal.

45. (New) The system of claim 39 wherein the at least two analog signals are substantially equal to each other.

46. (New) The system of claim 39 wherein the at least two analog signals are not substantially equal to each other.

47. (New) A system as in any of claims 17 or 39, wherein the signal conditioning stage generates a signal that is responsive to both the first analog signal and the second analog signal.

48. (New) A system as in any of claims 17 or 39, wherein the signal conditioning stage generates a signal that is responsive to each of the at least two of the at least two analog signals.